K.S. SCHOOL OF ENGINEERING AND MANAGEMENT, BANGALORE - 560109
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
SESSION: 2022-2023 (ODD SEMESTER)

SECOND ASSIGNMENT

Degree : B.E
Branch : Computer Science & Engineering
Course Title : Computer Organization & Architecture
Date : 20/1/2023

Semester : III
Course Code : 21CS34
Max Marks : 10
Last Date for Submission : 27/1/2023

Q No.	Question	Marks	K-Level	CO mapping
1	**Expand upon** the differences between parallel and serial port.	1	Understanding K2	CO2
2	**Explain** the functioning of serial port.	1	Understanding K2	CO2
3	**Outline** on privilege exception.	1	Understanding K2	CO2
4	**Elaborate** upon Centralized bus arbitration.	1	Understanding K2	CO2
5	**Interpret** upon Virtual address and physical address.	1	Understanding K2	CO3
6	**Discuss** the functions of Rambus memory	1	Understanding K2	CO3
7	**Elaborate on** Memory controller.	1	Understanding K2	CO3
8	**Discuss** flash memory briefly	1	Understanding K2	CO3
9	**Explain** the concept of MFC.	1	Understanding K2	CO3
10	**Restate** the usage of static RAM'S	1	Understanding K2	CO3

Supriya M
Course Incharge

HOD 20/1/23

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QUESTION BANK-1

Computer Organization and Architecture(21CS34)

Module-1

1. Explain basic operational concepts
2. Explain the types of buses with examples
3. Explain the performance measure of a system
4. Explain SPEC Rating
5. Explain a) Byte addressability b) Big-Endian c)Little – Endian
6. Explain the basic instruction types with examples.
7. What are condition codes, explain with examples
8. Explain all the addressing modes with examples
9. Explain indexing supported with a program
10. Write a program using one-address, two-address and three-address for A*B + C*D
11. Generate the effective addresses for the following- a) LOAD 20(R2), R0 b) MOV #2000, R0 c) ADD -R1, R2 (Hint- Use the staring address as some value say 1000, from there calculate the effective address whether using Immediate/ Relative etc)

Module-2

1. Explain the basic Input/output organization.
2. Write a brief on interrupts with an example
3. Elaborate on the interrupt hardware
4. With neat sketches explain various methods to handle multiple interrupts raised by multiple devices
5. Explain the scenario when the interrupts are enabled.
6. Explain exception and the different kinds.
7. With respect to the operating system, explain how the interrupts are handled
8. Explain DMA with an example
9. Explain bus arbitration, support it with examples.
10. Explain synchronous and asynchronous buses with drawbacks highlighted.
11. Explain the parallel port interface with a) Keyboard b) Printer
12. Explain Serial port, support it with a example

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QUESTION BANK-2

Computer Organization and Architecture(21CS34)

Module-2

1. **Elaborate** on bus arbitration, support it with examples.
2. **Discuss** synchronous and asynchronous buses with drawbacks highlighted.
3. **Outline** the parallel port interface with a) Keyboard b) Printer.
4. **Explain** Serial port, support it with a example.
5. **Discuss** Parallel port with the timing logic introduced and what is the advantage in introducing the same.
6. **Expand uponmultiple** cycle transfers in Synchronous Bus.

Module-3

1. **Discuss** the concept of MFC in main memory organization.
2. **Explain** a) Physical address b) Logical address c) Flash memory d) Rambūs Memory e) Memory Controller.
3. **Interpret** the internal organization of memory chips.
4. **Outline** a) SRAM b) Asynchronous DRAM c)Synchronous DRAM .
5. **Interpreton** ROM and its types.
6. **Demonstrate** the mapping functions in Cache.
7. **Discuss** replacement algorithm with an example .
8. **Illustrate** refresh overhead with an example.

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QUESTION BANK-3

Computer Organization and Architecture(21CS34)

Module 4-

1. **Calculate** the summation of signed numbers -7 and +1 in binary
2. **Draw** a full adder and show its working.
3. **Illustrate** a carry look ahead adder with its working with an example.
4. **Demonstrate** the working of multiplication of binary numbers with its working, with an example.
5. **Demonstrate** a datapath with the instruction set processor.
6. **Exercise** the working of a complete instruction for ADD R3, R1
7. **Exhibit** the fetching a word from memory with respect to MDR.
8. **Draw** a data path with respect to multiple bus organization.
9. **Exhibit** the working of hardwired control.
10. **Construct** a micro-program sequence for ADD Rsrc, Rdst using F1 to F8 groups.
11. **Construct** a micro-program sequence for unconditional branch or b it-ORing for ADD Rsrc, Rdst using next address field.

Module 5

1. **Figure out** the Flynn's classification for which it divides the computer into four major groups.
2. **Construct** the pipeline sequence for $(a_i - b_i)/c_i + d_i$
3. **Demonstrate** the working of arithmetic pipeline for $x = 0.9504*10^3$ and $y = 0.0820*10^3$ with t1, t2, t3, t4 as 60ns, 70ns, 100ns, 80ns respectively.
4. **Demonstrate** an instruction pipeline for sequence of 9 instructions with after 4^{th} instruction there is a BRANCH.
5. **Provide** the methods to handle BRANCH instructions.
6. **Exhibit** a) Vector processor for matrix multiplication b) Array Processor